7.6 A High-Speed Back-Illuminated Stacked CMOS Image Sensor with Column-Parallel kT/C-Cancelling S&H and Delta-Sigma ADC

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In recent years, there has been growing demand for high-resolution and large-format CMOS image sensors in Digital Still Camera, Security, and Factory Automation uses. In addition, new uses such as airborne mapping [1] are now being reported. Focusing on the camera market, there is currently demand for simultaneously realizing high image quality, high frame rate, and low power consumption, all within a larger-than-APS-C format. For most cases, the single-slope ADC (SS ADC) [2] architecture is used in commercialized CMOS image sensors. In order to accelerate frame rate, the counting-clock frequency can be increased up to 2.376GHz as demonstrated in [3], but maintaining clock waveform quality without increasing power is a major challenge for low-power operation. Adaptive gain operation using a dual gain amplifier is reported in [4], but SS ADCs based on adaptive gain operation still have frame rate issues from increasing bit resolution, e.g., to 14b.

This paper presents a 50.1Mpixel 250fps back-illuminated (BI) stacked CMOS image sensor realizing as low as 1.18e-rms random noise (RN) at 0dB even in the large format. To keep the high resolution, high speed, and high image quality, we apply the following three technologies shown in Fig. 7.6.1: (1) Split-pixel signal line for lowering the wiring load and increasing the operation speed; (2) Pipelined operation for high speed, kT/C noise cancelling sample & hold (S&H), and adaptive gain control for low noise; and (3) delta-sigma ADC for high speed and high resolution.

Figure 7.6.1 also shows a block diagram of the sensor. This sensor consists of a pixel array, column-parallel S&Hs and delta-sigma ADCs, logic blocks for the signal processing and data output rate conversion, and an 8-lane Scalable Low Voltage Signaling interface with Embedded Clock (SLVS-EC). Furthermore, we use Cu-Cu connection technology for the signal connection between the upper and lower chip, which enables narrower pitch and splits the signal line underneath the center area of pixels. Total pixel count is 50.1Mpixels and the pixel pitch is 4.16μm. The process node is 90nm MOS for the upper chip and 40nm CMOS for the lower chip.

Figure 7.6.2 shows the column-parallel kT/C noise-cancelling S&H and delta-sigma ADC circuit. Two pairs of S&H circuits are used for the Reset phase (Φ_R) and Signal phase (Φ_S), and then the S&H's outputs are subtracted in "Analog-CDS" manner. Moreover, there are two sets of these S&H pairs (total 4 S&Hs on each signal line) used in pipelined operation, as shown in Fig. 7.6.3.

The Read phase has the function of readout and sampling of pixel signal, kT/C noise cancellation and a signal level judgement for adaptive gain control (AGC). The S&H circuit realizes not only pipelined operation for the fast readout, but also kT/C noise cancellation using a negative capacitance feedback during the kT/C noise-cancellation period. Although [5] and [6] report a kT/C cancellation technique as a cancellation at the output, we report kT/C cancellation where the cancelling occurs at the input, because it has better compatibility with the flip-around type S&H. At first, auto-zero operates by turning both SW1 and SW2 on; then, the pixel signal level is sampled on C_{sample} by turning SW2 off. At this time, kT/C noise, charge injection, and clock feedthrough are also sampled to generate a deviation from the auto-zero level. But after SW3 is turned on, the negative feedback loop comprised of C_{fb1}, C_{fb2}, and C_{fb3} makes this deviation return to the original auto-zero level; in this way, the kT/C noise is cancelled. The kT/C noise of SW3 when it is turned off is negligible because this noise is reduced by a second capacitance divider using C_{fb1}, C_{fb2}, and C_{fb3}. This series of operations is executed during the kT/C cancellation period of Φ_R and Φ_S. During the last part of the Read-phase, the pixel signal level judgement for AGC compared to 1/8 (=0.125) of the sensor full-scale is done. This judgement result is used for selecting the gain setting in consecutive ADC phases to lower the RN of the low-illuminance portion.

The ADC phase has the function of analog CDS and ADC. Four columns of the S&H's analog CDS outputs are shared by one delta-sigma ADC in a time-division manner, as also shown in Fig. 7.6.3. The analog CDS is realized by a voltage-to-current conversion resistor (R) placed between two outputs of S&H, and its analog gain is controlled by changing the resistor value that is properly selected by the level judgement operation of the AGC. As for the ADC, a current-input 2nd-order continuous-time (CT) delta-sigma ADC is adopted. According to the signal level, I_{signal} is integrated by a capacitor on the first stage and then integrated again by the g_m and capacitor on the second stage. After that, a 1b quantized result is used as the output and is fed back to the current DAC of the first and second stages. Finally, the result is converted to a 14b output by using the decimation filter. Although the ADC uses a 2nd-order delta-sigma modulator, it is simplified by using the current output from the analog CDS as the first integrator output. Further, the adopted AGC in front of the delta-sigma ADC relaxes the fixed pattern noise (FPN), RN, and power consumption. The analog-to-digital conversion result is transferred to the signal-processing block together with the AGC judgement result, and is reconstructed while being divided by 8 when the signal level is below 1/8 of the full scale to realize on-chip AGC operation. Finally, on-chip calibration that calculates a compensation coefficient during the vertical blanking period can also improve the reconstructed linearity at the AGC boundary and the vertical FPN.

Figure 7.6.4 shows the evaluated sensor linearity and the reconstructed sample image compares a frame rate of 30fps with 250fps, indicating the rolling shutter distortion. The resolution of gain-adaptive column ADCs is 14b. The output code obtained by high gain is divided by the AGC gain ratio in the subsequent digital block, where the linear 14b outputs are reconstructed with nonlinearity within -0.42% of the full scale without any special trimming.

Figure 7.6.5 is the chip micrograph showing a sensor chip and a logic chip. Figure 7.6.6 summarizes the chip characteristics. The sensor achieves 1.18e-rms RN at 0dB. The row temporal noise without compensation and the vertical FPN with on-chip compensation are measured to be 0.04e-rms and 0.04e-rms, respectively, at an analog gain of 0dB. The total output rate of 44fps is defined as "Frame rate", and the ADC readout rate of the effective pixel area reading time is 250fps and defined as "Readout rate".

In summary, due to the pipelined operation with the column-parallel kT/C cancelling S&H, high-speed delta-sigma ADC architecture, and the split pixel line technology, we achieve 50.1Mpixel 14-bit 250fps readout rate and 44fps frame rate; power consumption is 2760mW including on-chip calibration and compensation. Figure 7.6.7 shows a performance comparison table among [4,7-9] and the FoM6 [e-*pJ/step] comparison in recent papers showing this work achieves state-of-the-art performance.

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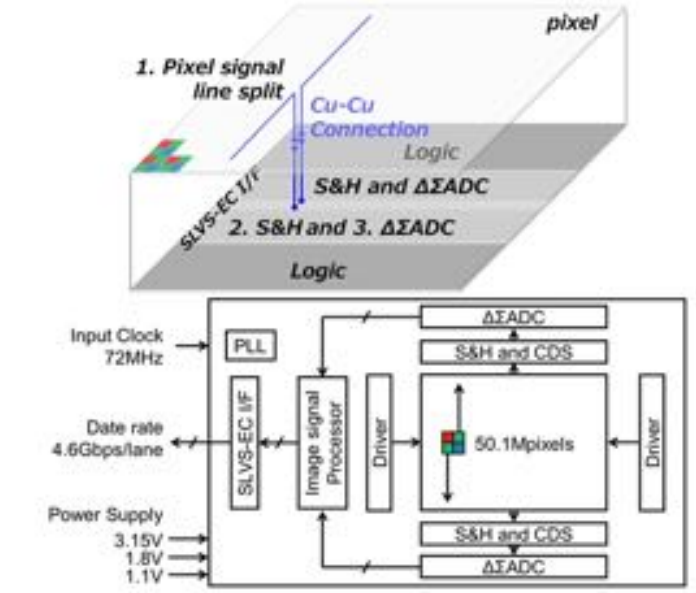

Figure 7.6.1: 3 key technologies and block diagram of the sensor.

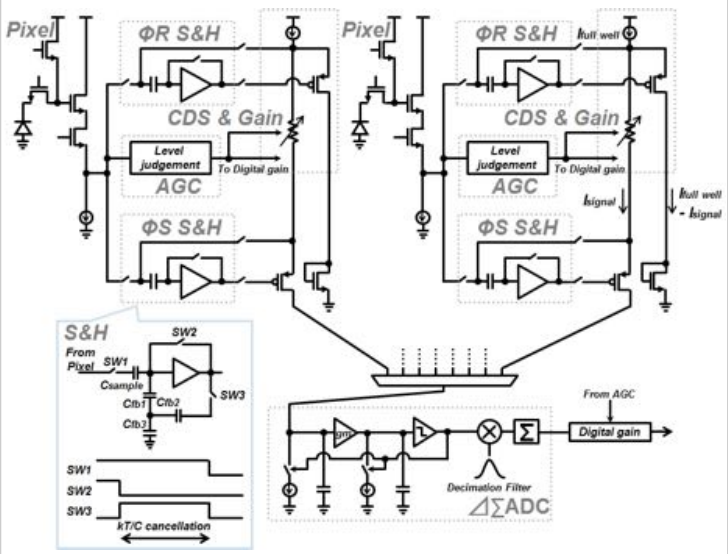

Figure 7.6.2: Column-parallel kT/C-cancelling S&H and delta-sigma ADC circuit.

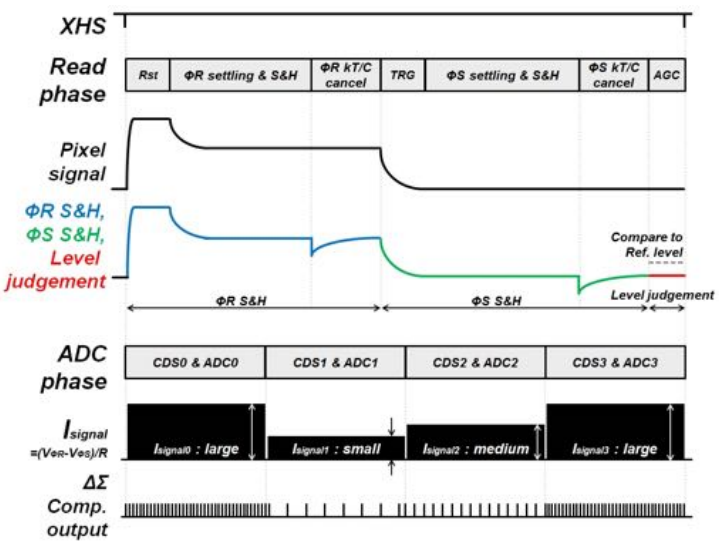

Figure 7.6.3: Timing diagram of a horizontal scanning period.

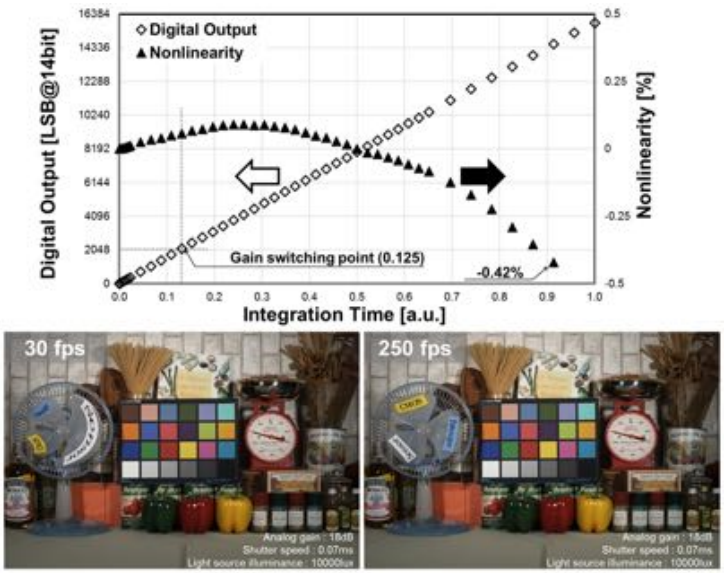

Figure 7.6.4: Sensor linearity and reconstructed image with RS distortion.

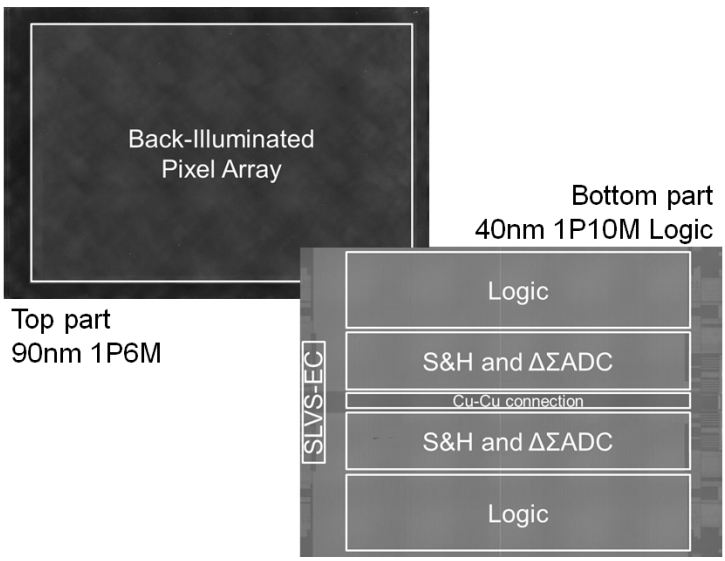

Figure 7.6.5: Chip micrograph of a sensor chip and a logic chip.

Fabrication process	90nm 1P6M; 40nm 1P10M logic
Supply voltage	3.15V / 1.8V / 1.1V
Pixel size	4.16μm(H) x 4.16μm(V)
Pixel number	50.1Mpixels
Output interface	8lane x 4.6Gbps/lane SLVS-EC
Conversion gain	85.7μV/e-
RMS random noise	1.18e-rms@0dB
Row temporal noise	0.04e-rms@0dB
Vertical FPN	0.04e-rms@0dB w/ on-chip compensation
Frame rate	44fps
Readout rate	250fps@14bit
Power consumption	2760mW@14bit, 44fps

Figure 7.6.6: Chip characteristics.

	ISSCC 2016 [4]	ISSCC 2015 [7]	VLSI 2016 [8]	ISSCC 2018 [9]	This work
Shutter operation	RS	RS	GS	GS	RS
ADC resolution [bit]	12	14	14	14	14
Number of pixel [Mpixels]	251.4	135.9	8.3	1.5	50.1
Frame rate [fps]	5	60	480	660	44
Analog gain [times]	1	2	1	1	1
Random noise [e⁻rms]	3.5	7.68	4.62	5.15	1.18
Power [mW]	1970	11050	5230	746	2760
FoM1 [e⁻/MHz]	54.89	14.59	4.46	8.71	4.63
FoM6 [e⁻·pJ/step]	1.34	0.64	0.37	0.24	0.09

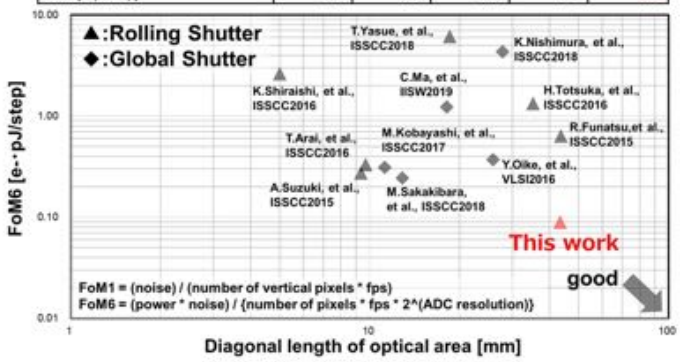

Figure 7.6.7: Performance and FoM6 [e-*pJ/step] comparison.

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